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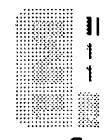
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**1 Engineering dynamic real-time distributed systems: architecture, system description language, and middleware**

*Ravindran, B.;*

Software Engineering, IEEE Transactions on , Volume: 28 , Issue: 1 , Jan. 200  
Pages:30 - 57

[\[Abstract\]](#) [\[PDF Full-Text \(561 KB\)\]](#) [IEEE JNL](#)

**2 Distributed audit trail analysis**

*Mounji, A.; Le Charlier, B.; Zampunieris, D.; Habra, N.;*

Network and Distributed System Security, 1995., Proceedings of the Symposium on , 16-17 Feb. 1995  
Pages:102 - 112

[\[Abstract\]](#) [\[PDF Full-Text \(844 KB\)\]](#) [IEEE CNF](#)

**3 A next generation expert system for flexible assembly**

*Rubin, S.H.;*

Systems Engineering, 1992., IEEE International Conference on , 17-19 Sept. 1  
Pages:393 - 398

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**4 Merging voice communications and information processing: using a platform for voice information services**

*McAllister, M.J.; Jackson, A.L.;*

Computers and Communications, 1990. Conference Proceedings., Ninth Annual International Phoenix Conference on , 21-23 March 1990  
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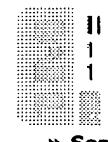
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**1 Retargeting Web pages to other computing platforms with VAQUIT***Bouillon, L.; Vanderdonckt, J.;*  
Reverse Engineering, 2002. Proceedings. Ninth Working Conference on , 29 Oc Nov. 2002

Pages:339 - 348

[\[Abstract\]](#) [\[PDF Full-Text \(580 KB\)\]](#) [IEEE CNF](#)**2 A language for software subsystem composition***Buffenberger, J.; Gruell, K.;*  
System Sciences, 2001. Proceedings of the 34th Annual Hawaii International Conference on , 3-6 Jan. 2001

Pages:10 pp.

[\[Abstract\]](#) [\[PDF Full-Text \(320 KB\)\]](#) [IEEE CNF](#)**3 Towards automatic synthesis of QoS preserving implementations fr object-oriented design models***Saksena, M.;*  
Object-Oriented Real-Time Dependable Systems, 1999. Proceedings. Fifth International Workshop on , 18-20 Nov. 1999

Pages:93 - 99

[\[Abstract\]](#) [\[PDF Full-Text \(48 KB\)\]](#) [IEEE CNF](#)**4 Extracting parallelism in Fortran by translation to a single assignme intermediate form***Barry, R.J.; Evripidou, P.;*  
Parallel Processing Symposium, 1994. Proceedings., Eighth International , 26-

April 1994  
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**5 Predicting the performance of scientific applications on distributed memory multiprocessors**

*Abramson, D.;*

Scalable High-Performance Computing Conference, 1994. Proceedings of the , 25 May 1994

Pages:285 - 292

[\[Abstract\]](#) [\[PDF Full-Text \(540 KB\)\]](#) [IEEE CNF](#)

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Pages:125 - 136[\[Abstract\]](#) [\[PDF Full-Text \(352 KB\)\]](#) **IEEE JNL****2 Learning about digital signal processing using spreadsheets and simulation software***Baicher, G.S.; Sherrington, J.A.;*Engineering Science and Education Journal , Volume: 5 , Issue: 1 , Feb. 1996  
Pages:41 - 48[\[Abstract\]](#) [\[PDF Full-Text \(748 KB\)\]](#) **IEE JNL****3 Versatile real time microprocessor development system***Abdelbaki, H.E.M.;*

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Pages:C32 - 1-8

[\[Abstract\]](#) [\[PDF Full-Text \(491 KB\)\]](#) **IEEE CNF****4 Window theory of local image processing (IP): a framework for mapping local IP algorithms onto local IP systems under real time constraints***Theis, J.-P.;*

Parallel and Distributed Real-Time Systems, 1997. Proceedings of the Joint

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Pages:302 - 308

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**5 Cache memory design for embedded systems based on program loc analysis**

*Giorgi, R.; Prete, C.A.; Prina, G.;*

Microelectronic Systems Education, 1997. MSE '97. Proceedings., 1997 IEEE International Conference on , 21-23 July 1997

Pages:16 - 18

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**6 The real-time functional test facility for advanced instrumentation a control in nuclear power plants**

*Kee-Choon Kwon; Soon-Ja Song; Won-Man Park; Sung-Pil Lyu;*

Nuclear Science, IEEE Transactions on , Volume: 46 , Issue: 2 , April 1999

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**7 A 1.2-W, 2.16-GOPS/720-MFLOPS embedded superscalar microprocessor for multimedia applications**

*Kubosawa, H.; Takahashi, H.; Ando, S.; Asada, Y.; Asato, A.; Suga, A.; Kimura, M.; Higaki, N.; Miyake, H.; Sato, T.; Anbutsu, H.; Tsuda, T.; Yoshimura, T.;*

*Amano, I.; Kai, M.; Mitarai, S.;*

Solid-State Circuits, IEEE Journal of , Volume: 33 , Issue: 11 , Nov. 1998

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**8 Fine grain mapping strategy for multiprocessor systems**

*Shieh, J.J.; Papachristou, C.A.;*

Computers and Digital Techniques, IEE Proceedings E [see also Computers and Digital Techniques, IEE Proceedings-] , Volume: 138 , Issue: 3 , May 1991

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**9 Environment for multiprocessor simulator development**

*Wakabayashi, M.; Amano, H.;*

Parallel Architectures, Algorithms and Networks, 2000. I-SPAN 2000. Proceedings International Symposium on , 7-9 Dec. 2000

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**10 Development of the test simulator for advanced instrumentation a control research**

*Kee-Choon Kwon; Soon-Ja Song; Won-Man Park; Jang-Soo Lee; Jang-Yeol Kim*

Human Factors and Power Plants, 1997. 'Global Perspectives of Human Factor Power Generation', Proceedings of the 1997 IEEE Sixth Conference on , 8-13

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**11 System design using ASIPs**

*Carro, L.; Pereira, G.A.; Alba, C.; Suzim, A.;*  
Engineering of Computer-Based Systems, 1996. Proceedings., IEEE Symposium  
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**12 A design framework of interactive distance learning in distributed systems**

*Kamolphiwong, T.; Kamolphiwong, S.; Siriyuenyong, C.;*  
Computers in Education, 2002. Proceedings. International Conference on, 3-6  
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**13 Performance modeling for adaptive parallel embedded systems**

*Asaad, S.; Bapty, T.;*  
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International, 3-5 April 2002  
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**14 A design framework to efficiently explore energy-delay tradeoffs**

*Fornaciari, W.; Sciuto, D.; Silvano, C.; Zaccaria, V.;*  
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International Symposium on, 25-27 April 2001  
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**15 Design and simulation of a RISC-based 32-bit embedded on-board computer**

*Zhen Guo; He Li; Shuling Guo; Dongsheng Wang;*  
Test Symposium, 1998. ATS '98. Proceedings. Seventh Asian, 2-4 Dec. 1998  
Pages:413 - 416

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